METHOD AND APPARATUS FOR DEBUGGING A CHIP

ABSTRACT

In a first aspect, an apparatus is provided that is adapted to multiplex debug signals of an integrated circuit. The apparatus includes at least a first multiplexing circuit and a second multiplexing circuit. The first multiplexing circuit is adapted to receive first debug signals from the integrated circuit and to selectively multiplex at least a first portion of the first debug signals onto a first bus. The second multiplexing circuit is adapted to receive second debug signals from the integrated circuit and to selectively multiplex at least a first portion of the second debug signals onto a second bus. The apparatus further includes a logic circuit adapted to combine any debug signals of the first and second buses onto a third bus. An output stage of the apparatus is adapted to selectively output debug signals of the third bus. Numerous other aspects are provided, as are systems and methods.